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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/942,116	08/29/2001	William R. Wheeler	10559/601001/P12885	6930

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EXAMINER	
FERRIS III, FRED O	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/942,116	WHEELER ET AL.	
	Examiner	Art Unit	
	Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-8 and 10-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3, 5-8, and 10-15* is/are allowed.

6)☒ Claim(s) *16-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10 February 2006 has been entered. Claims 1-3, 5-8, and 10-24 remain pending in this application. Of these, claims 1-3, 5-8, and 10-15 have now been allowed over the prior art of record. Claims 16-24 remain rejected.

Response to Arguments

2. Applicant's arguments filed 10 February 2006 have been fully considered.

Regarding applicant's response to 103(a) rejections: The examiner now withdraws the 103(a) rejection of claims 1-3, 5-8, and 10-15 in view of applicant's amendment to the claims. (See allowable subject matter below) However, the examiner maintains the claims 16-24 remain obvious in view of the prior art of record. Specifically, while the examiner concurs with applicants arguments that Jain and Bushard do not explicitly disclose the same combination of three bits for indicating a particular condition representing the state of the node, the examiner maintains that the disclosed technique merely amounts to "bit mapping" of the four possible node states. Bushard, for example, clearly discloses using such bit mapping techniques for changing (and representing) state values during simulation (CL9-L1-15). (Also see: "bit

map"/"pattern", Microsoft Computer Dictionary, Third Edition, 1997) Bushard further teaches that such techniques are "known" to one skilled in the art (CL9-L3). Hence, a skilled artisan having access to the teachings of Bushard, or simply being familiar with well-known bit mapping techniques, would have knowingly implemented the logic design by storing three bits of state information for a node representing the possible values of state and logic as a method for bit mapping and storing the state and logic values. Relating to claims 22-24, applicants argue that Wang fails to teach copying the instruction to a second page and executing the second page starting with the instruction as recited in claims 22-24. The examiner asserts that this feature is necessarily obvious in view of Wang because Wang teaches copying to computer executable instructions (abstract) into secondary pages (CL1-L55-CL2-L7, Figs. 5-7) as part of the write protecting process. Hence a skilled artisan having access to the teachings of Wang would have known to execute the stored instructions from the second memory page out of necessity as part of the write protection process using the reasoning previously cited below under 103(a) rejections. Accordingly, the examiner has maintained the rejection of claims 16-24.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,044,211 issued to Jain in view of U.S. Patent 5,819,072 issued to Bushard et al.

Regarding independent claim 16: Jain discloses the simulation of a logic design (Figs. 4-6) inclusive of identifying and storing the state(s) of the node (CL13-L16-21, CL24-L17-26) and determining the output of the node (CL5-L55-59, CL24-L29) during simulation based on value(s) of the prior state(s) (CL21-L29-33, 50, 61-63). Hence, Jain renders obvious the elements of the limitations relating to storing and identifying multiple node states (i.e. first, second, third, etc.) based on a logic value. (Tabs. II-IV, Fig. 5) This claim merely requires storing three bits of state information, and then subsequently checking the three bits in simulating operation of the logic design. The examiner further notes that storing the state information as three bits representing to possible node states merely amounts to bit pattern mapping of the state values and hence would have been knowingly implemented by a skilled artisan (see: bit map/pattern, Microsoft Computer Dictionary, Third Edition, 1997).

Jain does not explicitly disclose four state simulation. (i.e. state values of, high, low, high impedance, and undefined).

Bushard teaches a four state simulator (CL8-L66-67, CL9-L4, 21-22, and 59-61) where the possible values include high (1), low (0), high impedance (unknown), and undefined (don't care). (CL9-L31-37, 57-65, Figs. 7, 8) Determining if the simulation was "successful" based on the state of the output node is obvious in view of Bushard because Bushard teaches a four state simulation that identifies and stores the state values, and then subsequently analyzes the circuit design based these values (CL10-L3-15, i.e. high, low, unknown, etc.). Hence a skilled artisan having access to the teachings of Bushard would have known to use state values (i.e. four states, high, low, high impedance, and undefined, in determining if the simulation of the logic was successful. Here, the term the term "successful" simply implies that no "undefined states" were determined during simulation as disclosed in applicant's specification, page 8, line 13. This feature is therefore rendered obvious by Bushard because Bushard teaches detecting (determining) if a simulation contains any unknown (i.e. undefined, not initialized) logic states and then storing the unknown states in a list (CL10-L9-11). Obviously, if no undefined states are determined during simulation, a four state simulation is simply not required since a four state simulation is only needed if undefined (i.e. forth state) logic values exist. The specification (page 9, line 6) appears to reinforce this reasoning.

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Jain relating to simulation of a

logic design and identifying and storing node state values, with the teachings of Bushard relating to the use of multi-state values in logic design simulation, to realize the claimed invention. An obvious motivation exists since, in this case, the Jain reference teaches to the Bushard reference, and the Bushard reference teaches to the Jain reference. Specifically, both Jain and Bushard teach simulation of a logic designs and are used in the same technical arena as noted above. Jain teaches to Bushard because Jain discloses that node values can be detected and stored for a given state. (See: Jain, CL13-L16-21). Bushard teaches to Jain because Bushard specifically discloses using multi-state values in logic design simulation. (See: Bushard, CL9-L27-67, Figs. 7, 8) Further, the level of skill required by an artisan to realize the claimed limitations of the present invention is clearly established by both references. (See: Jain/Bushard, Abstracts) Accordingly, a skilled artisan tasked with implementing a method of storing the states of logic simulation, and having access to the teachings of Jain and Bushard, would have knowingly modified the teachings of Jain with the teachings of Bushard (or visa versa) to realize the claimed elements of the present invention.

Per dependent claims 17-21: Bushard discloses determining the stored state/node value (high, low, etc.) based on up to four bits (CL9-L27-67, Figs. 7, 8) and considers undermined states and high impedance states and hence would have been knowingly implemented by a skilled artisan using the reasoning cited above.

4. Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,466,898 issued to Chan in view of U.S. Patent 6,738,875 issued to Wang.

Per independent claim 22: Chan teaches a cycle-based simulation (CL1-L45-57, CL2-L5-21, Figs. 3, 8, 11) of a logic design inclusive of logic computation instructions (CL4-L5-19, Tab. 1) and multiple memory pages (CL8-L13-24).

Chan does not explicitly disclose a write-protected memory.

Wang teaches techniques for write protecting a memory page, copying to secondary pages, un-protecting a write-protected page, rewriting values, and re-protecting the original write protected page. (CL1-L55-CL2-L7, Figs. 5-7)

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Chan relating to a cycle-based simulation, with the teachings of Wang relating to write protecting memory pages, to realize the claimed invention. An obvious motivation exists since this area of technology is highly competitive with many cycle-based simulation tools available in the market place and large amounts of money being spent in product development and improvement. (See: Wang, Table 1, for example) Accordingly, a skilled artisan would have made an effort to become aware of what capabilities had already been developed in the market place and, hence, would have knowingly modified the teachings of Chan with the teachings of Wang in order to reduce development time and cost.

Per dependent claims 23-24: These claims merely require inserting an illegal instruction into the memory page to trigger an exception to the write protection process.

This technique is well known in the art and would have knowingly been used by a skilled artisan as a method of generating a processor interrupt for handling write protection routine. (See: definition for "exception", Microsoft Computer Dictionary", Third Edition, 1997)

Allowable Subject Matter

5. The following is a statement of reasons for the indication of allowable subject matter: Independent claims 1, 6, and 11 include a specific sequence of method steps and arrangement of apparatus elements that includes storing of a first, second, and third state based respectively upon the identification of a simulation logic design node having a high, low, and undefined state value, and subsequently performing a three states simulation based the three states, and further upon the determination of a successful three state simulation, and based on whether the output node has an undefined state with the three state simulation being successful if the output node is a defined state performing a four state simulation of the logic design, which is not explicitly disclosed or rendered obvious by the prior art of record.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Careful consideration should be given prior to applicant's response to this Office Action.

U.S. Patent 6,718,522 issued to Mc Bride et al teaches simulating logic design and storing node state values.

"Process-Level Modeling with VHDL", J. Armstrong, Proceeding Verilog HDL Conference, March 1998, IEEE teaches simulating logic design and storing node state values.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached at 571-272-2279. The Official Fax Number is: (703) 872-9306

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April 27, 2006

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